II. Listing of Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Presently Amended) A microelectronic device, comprising:

~~an insulator located over a substrate;~~

~~a semiconductor feature located over the insulator and having a thickness, a first surface opposite the insulator, and a sidewall spanning at least a portion of the thickness; and~~

~~a contact layer having a first member extending over at least a portion of the first surface and a second member spanning at least a portion of the sidewall~~

an insulator extending over at least a portion of a substrate;

a semiconductor feature extending over at least a portion of the insulator; and

a contact layer having a first portion connecting a second portion and a third portion, wherein the first contact layer portion spans a sidewall of the semiconductor feature, and wherein a portion of the semiconductor feature interposes and contacts the second and third contact layer portions.

Claims 2-4. (Cancelled).

5. (Presently Amended) The device of claim 1 wherein the third contact layer portion interposes at least ~~comprises a third member connected to the second member and interposing~~ a portion of the insulator and at least a portion of the semiconductor feature.

6. (Presently Amended) The device of claim 5 wherein the third ~~member of the~~ contact layer portion has a thickness of at least about 10 Angstroms.

7. (Original) The device of claim 1 wherein the contact layer comprises metal.

8. (Original) The device of claim 1 wherein the contact layer comprises metal silicide.

9. (Original) The device of claim 1 wherein the contact layer comprises cobalt silicide.

10. (Original) The device of claim 1 wherein the contact layer comprises nickel silicide.

11. (Original) The device of claim 1 wherein the contact layer comprises metal nitride.

12. (Original) The device of claim 1 wherein the contact layer comprises metal oxide.

13. (Presently Amended) The device of claim 1 wherein ~~the first member~~ at least one of the first, second and third portions of the contact layer has a thickness of less than about 400 Angstroms.

14. (Original) The device of claim 1 wherein the semiconductor feature comprises silicon.

15. (Original) The device of claim 1 wherein the semiconductor feature comprises silicon and germanium.

16. (Original) The device of claim 1 wherein the semiconductor feature comprises silicon and carbon.

17. (Original) The device of claim 1 wherein the semiconductor feature comprises silicon, germanium and carbon.

18. (Original) The device of claim 1 wherein the semiconductor feature has a thickness of at least about 400 Angstroms.

19. (Original) The device of claim 1 wherein the semiconductor feature has a thickness of at least about 100 Angstroms.

20. (Original) The device of claim 1 wherein the insulator comprises an oxide.

21. (Original) The device of claim 1 wherein the insulator comprises silicon nitride.

22. (Original) The device of claim 1 wherein the insulator comprises silicon oxynitride.

23. (Original) The device of claim 1 wherein the insulator comprises a high-k dielectric material.

24. (Original) The device of claim 1 wherein the insulator comprises a buried oxide layer.

25. (Original) The device of claim 1 wherein the substrate is a silicon-on-insulator (SOI) substrate having an insulating layer interposing a semiconductor layer and a bulk substrate, the insulator is defined in the insulating layer, and the semiconductor feature is defined in the semiconductor layer.

26. (Presently Amended) A transistor device, comprising:

an insulator located over a substrate;

a gate located over the insulator;

source and drain regions located over the insulator and on opposing sides of the gate ~~and having a thickness over the insulator, each of the source and drain regions having a first surface opposite the insulator and a sidewall distal from the gate and spanning at least a portion of the thickness~~; and

source and drain contacts each having a first ~~member extending over at least a portion of a corresponding first surface and a second member spanning at least a portion of a corresponding sidewall~~ portion connecting a second portion and a third portion, wherein the first portion spans a sidewall of a corresponding one of the source and drain regions, and wherein a portion of each of the source and drain regions interposes and contacts the second and third portions of the corresponding one of the source and drain contacts.

Claims 27-30. (Cancelled).

31. (Presently Amended) The device of claim 26 wherein the third ~~member~~ portion of each of the source and drain contacts has a thickness of at least about 10 Angstroms.

32. (Original) The device of claim 26 wherein at least one of the source and drain contacts comprises metal.

33. (Original) The device of claim 26 wherein at least one of the source and drain contacts comprises metal silicide.

34. (Presently Amended) The device of claim 26 wherein ~~the contact layer~~ at least one of the source and drain contacts comprises cobalt silicide.

35. (Presently Amended) The device of claim 26 wherein ~~the contact layer~~ at least one of the source and drain contacts comprises nickel silicide.

36. (Original) The device of claim 26 wherein at least one of the source and drain contacts comprises metal nitride.

37. (Original) The device of claim 26 wherein at least one of the source and drain contacts comprises metal oxide.

38. (Presently Amended) The device of claim 26 wherein ~~the first member~~ at least one of the first, second and third portions of at least one of the source and drain contacts has a thickness of less than about 400 Angstroms.

39. (Original) The device of claim 26 wherein at least one of the source and drain regions comprises silicon.

40. (Original) The device of claim 26 wherein at least one of the source and drain regions comprises silicon and germanium.

41. (Original) The device of claim 26 wherein at least one of the source and drain regions comprises silicon and carbon.

42. (Original) The device of claim 26 wherein at least one of the source and drain regions comprises silicon, germanium and carbon

43. (Original) The device of claim 26 wherein at least one of the source and drain regions has a thickness of at least about 400 Angstroms.

44. (Original) The device of claim 26 wherein at least one of the source and drain regions has a thickness of at least about 100 Angstroms.

45. (Original) The device of claim 26 wherein the insulator comprises an oxide.

46. (Original) The device of claim 26 wherein the insulator comprises silicon nitride.

47. (Original) The device of claim 26 wherein the insulator comprises silicon oxynitride.

49. (Original) The device of claim 26 wherein the insulator comprises a high-k dielectric material.

50. (Original) The device of claim 26 wherein the insulator is comprise a buried oxide layer.

51. (Presently Amended) A method of manufacturing a microelectronic device, comprising:

forming an insulator over a substrate;

forming a semiconductor feature ~~having a thickness over the insulator, a first surface opposite the insulator and a sidewall spanning at least a portion of the thickness~~ over at least a portion of the insulator; and

forming a contact layer having a first ~~member extending over at least a portion of the first surface and a second member spanning at least a portion of the sidewall~~ portion connecting a second portion and a third portion, wherein the first contact layer portion spans a sidewall of the semiconductor feature, and wherein a portion of the semiconductor feature interposes and contacts the second and third contact layer portions.

Claims 52-54. (Cancelled).

55. (Presently Amended) The method of claim 51 wherein the third contact layer portion interposes at least ~~includes a third member connected to the second member and interposing~~ a portion of the insulator and at least a portion of the semiconductor feature.

56. (Presently Amended) The method of claim 51 wherein the third ~~member of the~~ contact layer portion interposes the semiconductor feature and the insulator and has a thickness of at least about 10 Angstroms.

57. (Presently Amended) An integrated circuit device, comprising:

an insulator located over a substrate;

a plurality of microelectronic devices each including:

~~a semiconductor feature having a thickness over the insulator, a first surface opposite the insulator and a sidewall spanning at least a portion of the thickness; and~~

~~a contact layer having a first member extending over at least a portion of the first surface and a second member spanning at least a portion of the sidewall;~~

a semiconductor feature located over the insulator; and

a contact layer having a first portion connecting a second portion and a third portion, wherein the first contact layer portion spans a sidewall of the semiconductor feature, and wherein a portion of the semiconductor feature interposes and contacts the second and third contact layer portions;

a plurality of dielectric layers located over the plurality of microelectronic devices; and

a plurality of interconnects each extending through ones of the plurality of dielectric layers, at least one of the plurality interconnects interconnecting ones of the plurality of microelectronic devices.

58. (Presently Amended) The integrated circuit device of claim 57 wherein ~~a portion of each of the semiconductor features interposes the insulator and the second member of a corresponding contact layer~~ the third contact layer portion of each of the plurality of microelectronic devices interposes the insulator and the semiconductor feature of the corresponding one of the plurality of microelectronic devices.

59. (Presently Amended) The integrated circuit device of claim ~~57 wherein ones of the contact layers include comprise a third member connected to a corresponding second member and interposing a portion of the insulator and a portion of a corresponding semiconductor feature~~ 58 wherein the third contact layer portion of each of the plurality of microelectronic devices has a thickness of at least about 10 Angstroms.

60. (New) The method of claim 51 wherein the contact layer has a composition selected from the group consisting of:

metal;

metal silicide;

metal nitride; and

metal oxide.

61. (New) The method of claim 51 wherein the contact layer comprises a metal silicide selected from the group consisting of:

cobalt silicide; and

nickel silicide.

62. (New) The method of claim 51 wherein the semiconductor feature has a composition selected from the group consisting of:

a silicon composition;

a silicon and germanium composition;

a silicon and carbon composition; and

a silicon, germanium and carbon composition.

63. (New) The method of claim 51 wherein the insulator comprises at least one insulating material selected from the group consisting of:

oxide;

silicon nitride;

silicon oxynitride; and

high-k dielectric material.

64. (New) The method of claim 51 wherein forming the insulator includes forming a buried oxide layer in the substrate.

65. (New) The integrated circuit device of claim 57 wherein the contact layer of each of the plurality of microelectronic devices has a composition selected from the group consisting of:

metal;

metal silicide;

metal nitride; and

metal oxide.

66. (New) The integrated circuit device of claim 57 wherein the contact layer of each of the plurality of microelectronic devices comprises a metal silicide selected from the group consisting of:

cobalt silicide; and

nickel silicide.

67. (New) The integrated circuit device of claim 57 wherein the semiconductor feature of each of the plurality of microelectronic devices has a composition selected from the group consisting of:

a silicon composition;

a silicon and germanium composition;

a silicon and carbon composition; and

a silicon, germanium and carbon composition.

68. (New) The integrated circuit device of claim 57 wherein the insulator comprises at least one insulating material selected from the group consisting of:

oxide;

silicon nitride;

silicon oxynitride; and

high-k dielectric material.

69. (New) The integrated circuit device of claim 57 wherein the insulator is a buried oxide layer formed within the substrate.